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Cryo-CMOS Quantum-Classical Interfaces to Quantum Processors: from a Wild Idea to Working Silicon

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Abstract: The core of a quantum processor is generally an array of qubits that need to be controlled and read out by a classical processor. This processor operates on the qubits with nanosecond latency, several millions of times per second, with tight constraints on noise and power dissipation. This is due to the extremely weak signals from the processor that require highly sensitive circuits and systems, along with very precise timing capability. We advocate the use of CMOS technologies to achieve these goals, whereas the circuits will be operated at deep-cryogenic temperatures. We believe that these circuits, collectively known as cryo-CMOS control, will make future qubit arrays scalable, enabling a faster growth in qubit count. In this session, the challenges of modeling, designing, and operating complex circuits and systems at 4K and below will be outlined, along with preliminary results achieved in the control and read-out of qubits by *ad hoc* integrated circuits that were optimized to operate at low power in these conditions. We will conclude with a perspective on the field and its trends.

Organizer

Prof. Lodovico Ratti

Ph.D. Coordinators

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The seminar will take place in English.
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